VLSI TECHNOLOGY AND DESIGN

UNIT-I

VLSI Technology: Fundamentals and applications, IC production process, semiconductor processes, design rules and process parameters, layout techniques and process parameters.

VLSI Design: Electronic design automation concept, ASIC and FPGA design flows, SOC designs, design technologies: combinational design techniques, sequential design techniques, state machine logic design techniques and design issues.

UNIT-II

CMOS VLSI Design: MOS Technology and fabrication process of pMOS, nMOS, CMOS and BiCMOS technologies, comparison of different processes.

Building Blocks of a VLSI circuit: Computer architecture, memory architectures, communication interfaces, mixed signal interfaces.

VLSI Design Issues: Design process, design for testability, technology options, power calculations, package selection, clock mechanisms, mixed signal design.

UNIT-III

Basic electrical properties of MOS and BiCMOS circuits, MOS and BiCMOS circuit design processes, Basic circuit concepts, scaling of MOS circuits-qualitative and quantitative analysis with proper illustrations and necessary derivations of expressions.

UNIT-IV

Subsystem Design and Layout: Some architectural issues, switch logic, gate logic, examples of structured design (combinational logic), some clocked sequential circuits, other system considerations.
Subsystem Design Processes: Some general considerations and an illustration of design processes, design of an ALU subsystem.

UNIT-V

Floor Planning: Introduction, Floor planning methods, off-chip connections.

Architecture Design: Introduction, Register-Transfer design, highlevel synthesis, architectures for low power, architecture testing.

Chip Design: Introduction and design methodologies.

TEXT BOOKS:


REFERENCE BOOKS:


CMOS ANALOG IC DESIGN

UNIT –I


UNIT –II

Analog CMOS Sub-Circuits MOS Switch, MOS Diode, MOS Active Resistor, Current Sinks and Sources, Current Mirrors-Current mirror with Beta Helper, Degeneration, Cascode current Mirror and Wilson Current Mirror, Current and Voltage References, Band gap Reference.

UNIT –III

CMOS Amplifiers Inverters, Differential Amplifiers, Cascode Amplifiers, Current Amplifiers, Output Amplifiers, High Gain Amplifiers Architectures.

UNIT –IV


UNIT –V

Comparators Characterization of Comparator, Two-Stage, Open-Loop Comparators, Other Open-Loop Comparators, Improving the Performance of Open-Loop Comparators, Discrete-Time Comparators.
TEXT BOOKS:


REFERENCE BOOKS:


3. CMOS: Circuit Design, Layout and Simulation- Baker, Li and Boyce, PHI.
CPLD AND FPGA ARCHITECTURES AND APPLICATIONS

UNIT-I

Introduction to Programmable Logic Devices

UNIT-II

Field Programmable Gate Arrays
Organization of FPGAs, FPGA Programming Technologies, Programmable Logic Block Architectures, Programmable Interconnects, Programmable I/O blocks in FPGAs, Dedicated Specialized Components of FPGAs, Applications of FPGAs.

UNIT –III

SRAM Programmable FPGAs

UNIT –IV

Anti-Fuse Programmed FPGAs
Introduction, Programming Technology, Device Architecture, The Actel ACT1, ACT2 and ACT3 Architectures.

UNIT –V

Design Applications
General Design Issues, Counter Examples, A Fast Video Controller, A Position Tracker for a Robot Manipulator, A Fast DMA Controller, Designing Counters with ACT devices, Designing Adders and Accumulators with the ACT Architecture.
TEXT BOOKS:


REFERENCE BOOKS:

1. Field Programmable Gate Arrays - John V. Oldfield, Richard C. Dorf, Wiley India.


CMOS DIGITAL IC DESIGN

UNIT-I

MOS Design Pseudo NMOS Logic – Inverter, Inverter threshold voltage, Output high voltage, Output Low voltage, Gain at gate threshold voltage, Transient response, Rise time, Fall time, Pseudo NMOS logic gates, Transistor equivalency, CMOS Inverter logic.

UNIT-II

Combinational MOS Logic Circuits: MOS logic circuits with NMOS loads, Primitive CMOS logic gates – NOR & NAND gate, Complex Logic circuits design – Realizing Boolean expressions using NMOS gates and CMOS gates, AOI and OIA gates, CMOS full adder, CMOS transmission gates, Designing with Transmission gates.

UNIT-III

Sequential MOS Logic Circuits Behaviour of bistable elements, SR Latch, Clocked latch and flip flop circuits, CMOS D latch and edge triggered flip-flop.

UNIT-IV

Dynamic Logic Circuits Basic principle, Voltage Bootstrapping, Synchronous dynamic pass transistor circuits, Dynamic CMOS transmission gate logic, High performance Dynamic CMOS circuits.

UNIT-V

Semiconductor Memories Types, RAM array organization, DRAM – Types, Operation, Leakage currents in DRAM cell and refresh operation, SRAM operation Leakage currents in SRAM cells, Flash Memory- NOR flash and NAND flash.
TEXT BOOKS:


REFERENCE BOOKS:


DIGITAL SYSTEM DESIGN

UNIT-I

Minimization Procedures and CAMP Algorithm Review on minimization of switching functions using tabular methods, k-map, QM algorithm, CAMP-I algorithm, Phase-I: Determination of Adjacencies, DA, CSC, SSMs and EPCs, CAMP-I algorithm, Phase-II: Passport checking, Determination of SPC, CAMP-II algorithm: Determination of solution cube, Cube based operations, determination of selected cubes are wholly within the given switching function or not, Introduction to cube based algorithms.

UNIT-II

PLA Design, PLA Minimization and Folding Algorithms Introduction to PLDs, basic configurations and advantages of PLDs, PLA Introduction, Block diagram of PLA, size of PLA, PLA design aspects,

PLA minimization algorithm(IISc algorithm), PLA folding algorithm(COMPACT algorithm)-Illustration of algorithms with suitable examples.

UNIT-III

Design of Large Scale Digital Systems Algorithmic state machine charts-Introduction, Derivation of SM Charts, Realization of SM Chart, control implementation, control unit design, data processor design,

ROM design, PAL design aspects, digital system design approaches using CPLDs, FPGAs and ASICs.
UNIT-IV

Fault Diagnosis in Combinational Circuits Faults classes and models, fault diagnosis and testing, fault detection test, test generation, testing process, obtaining a minimal complete test set, circuit under test methods- Path sensitization method, Boolean difference method, properties of Boolean differences, Kohavi algorithm, faults in PLAs, DFT schemes, built in self-test.

UNIT-V

Fault Diagnosis in Sequential Circuits Fault detection and location in sequential circuits, circuit test approach, initial state identification, Haming experiments, synchronizing experiments, machine identification, distinguishing experiment, adaptive distinguishing experiments.

TEXT BOOKS:

1. Logic Design Theory-N. N. Biswas, PHI
3. Digital system Design using PLDd-Lala

REFERENCE BOOKS:

ADVANCED OPERATING SYSTEMS

UNIT-I

Introduction to Operating Systems Overview of computer system hardware, Instruction execution, I/O function, Interrupts, Memory hierarchy, I/O Communication techniques, Operating system objectives and functions, Evaluation of operating System

UNIT-II

Introduction to UNIX and LINUX Basic Commands & Command Arguments, Standard Input, Output, Input / Output Redirection, Filters and Editors, Shells and Operations

UNIT –III


Inter Process Communication: Introduction, File and record locking, Client – Server example, Pipes, FIFOs, Streams & Messages, Name Spaces, Systems V IPC, Message queues, Semaphores, Shared Memory, Sockets & TLI.

UNIT –IV

Introduction to Distributed Systems: Goals of distributed system, Hardware and software concepts, Design issues.

UNIT –V

Synchronization in Distributed Systems: Clock synchronization, Mutual exclusion, E-tech algorithms, Bully algorithm, Ring algorithm, Atomic transactions

Deadlocks: Dead lock in distributed systems, Distributed dead lock prevention and distributed dead lock detection.

TEXT BOOKS:

1. The Design of the UNIX Operating Systems – Maurice J. Bach, 1986, PHI.
2. Distributed Operating System - Andrew. S. Tanenbaum, 1994, PHI.

REFERENCE BOOKS:

UNIT –I

Introduction: Approaches to intelligent control, Architecture for intelligent control, Symbolic reasoning system, Rule-based systems, the AI approach, Knowledge representation - Expert systems.

UNIT –II

Artificial Neural Networks: Concept of Artificial Neural Networks and its basic mathematical model, McCulloch-Pitts neuron model, simple perceptron, Adaline and Madaline, Feed-forward Multilayer Perceptron, Learning and Training the neural network, Data Processing: Scaling, Fourier transformation, principal-component analysis and wavelet transformations, Hopfield network, Self-organizing network and Recurrent network, Neural Network based controller.

UNIT –III

Fuzzy Logic System: Introduction to crisp sets and fuzzy sets, basic fuzzy set operation and approximate reasoning, Introduction to fuzzy logic modeling and control, Fuzzification, inferencing and defuzzification, Fuzzy knowledge and rule bases, Fuzzy modeling and control schemes for nonlinear systems, Self-organizing fuzzy logic control, Fuzzy logic control for nonlinear time delay system.

UNIT –IV

Genetic Algorithm: Basic concept of Genetic algorithm and detail algorithmic steps, Adjustment of free parameters, Solution of typical control problems using genetic algorithm, Concept on some other search techniques like Tabu search and And-colony search techniques for solving optimization problems.
UNIT –V


TEXT BOOKS:


REFERENCE BOOKS:

DIGITAL DESIGN USING HDL

UNIT-I

Digital Logic Design using VHDL Introduction, designing with VHDL, design entry methods, logic synthesis, entities, architecture, packages and configurations, types of models: dataflow, behavioral, structural, signals vs. variables, generics, data types, concurrent vs. sequential statements, loops and program controls.

Digital Logic Design using Verilog HDL Introduction, Verilog Data types and Operators, Binary data manipulation, Combinational and Sequential logic design, Structural Models of Combinational Logic,

Logic Simulation, Design Verification and Test Methodology, Propagation Delay, Truth Table models using Verilog.

UNIT-II


Sequential Logic Circuit Design using VHDL Flip-flops, registers & counters, synchronous sequential circuits: Basic design steps, Mealy State model, Design of FSM using CAD tools, Serial Adder Example,

State Minimization, Design of Counter using sequential Circuit approach.

UNIT-III

Digital Logic Circuit Design Examples using Verilog HDL Behavioral modeling, Data types, Boolean-Equation-Based behavioral models of combinational logics, Propagation delay and continuous assignments, latches and level-sensitive circuits in Verilog, Cyclic behavioral
models of flip-flops and latches and Edge detection, comparison of styles for behavioral model; Behavioral model, Multiplexers, Encoders and Decoders, Counters, Shift Registers, Register files, Dataflow models of a linear feedback shift register, Machines with multi cycle operations, ASM and ASMD charts for behavioral modeling, Design examples, Keypad scanner and encoder.

UNIT-IV


UNIT-V

Testing of Digital Logic Circuits and CAD Tools Testing of logic circuits, fault model, complexity of a test set, path-sensitization, circuits with tree structure, random tests, testing of sequential circuits, built in self test, printed circuit boards, computer aided design tools, synthesis, physical design.

TEXT BOOKS:


REFERENCE BOOKS:


ADVANCED COMPUTER ARCHITECTURE

UNIT-I


UNIT-II

Pipelines Introduction, basic RISC instruction set, Simple implementation of RISC instruction set, Classic five stage pipe lined RISC processor, Basic performance issues in pipelining, Pipeline hazards, Reducing pipeline branch penalties.


UNIT-III

Instruction Level Parallelism (ILP)-The Hardware Approach

Instruction-Level parallelism, Dynamic scheduling, Dynamic scheduling using Tomasulo’s approach, Branch prediction, High performance instruction delivery-Hardware based speculation.

ILP Software Approach Basic compiler level techniques, Static branch prediction, VLIW approach, Exploiting ILP, Parallelism at compile time, Cross cutting issues - Hardware versus Software.
UNIT-IV

Multi Processors and Thread Level Parallelism Multi Processors and Thread level Parallelism- Introduction, Characteristics of application- domain, Systematic shared memory architecture, Distributed shared – Memory architecture, Synchronization.

UNIT-V

Inter Connection and Networks Introduction, Interconnection network media, Practical issues in interconnecting networks, Examples of inter connection, Cluster, Designing of clusters.

Intel Architecture Intel IA-64 ILP in embedded and mobile markets Fallacies and pit falls.

TEXT BOOKS:


REFERENCE BOOKS:


HARDWARE SOFTWARE CO-DESIGN

UNIT-I

Co- Design Issues Co- Design Models, Architectures, Languages, A Generic Co-design Methodology.

Co- Synthesis Algorithms Hardware software synthesis algorithms: hardware – software partitioning distributed system co-synthesis.

UNIT-II

Prototyping and Emulation Prototyping and emulation techniques, prototyping and emulation environments, future developments in emulation and prototyping architecture specialization techniques,

system communication infrastructure

Target Architectures Architecture Specialization techniques, System Communication infrastructure, Target Architecture and Application System classes, Architecture for control dominated systems (8051-

Architectures for High performance control), Architecture for Data dominated systems (ADSP21060, TMS320C60), Mixed Systems.

UNIT-III

Compilation Techniques and Tools for Embedded Processor Architectures Modern embedded architectures, embedded software development needs, compilation technologies, practical consideration

in a compiler development environment.
UNIT-IV:

Design Specification and Verification Design, co-design, the co-design computational model, concurrency coordinating concurrent computations, interfacing components, design verification, implementation verification, verification tools, interface verification.

UNIT-V:

Languages for System-Level Specification and Design-I

System-level specification, design representation for system level synthesis, system level specification languages.

Languages for System-Level Specification and Design-II

Heterogeneous specifications and multi language co-simulation, the cosyma system and lycos system.

TEXT BOOKS:


REFERENCE BOOKS:

VLSI LABORATORY-I

• The students are required to design the logic circuit to perform the following experiments using necessary simulator (Xilinx ISE Simulator/Mentor Graphics Questa Simulator) to verify the logical /functional operation and to perform the analysis with appropriate synthesizer (Xilinx ISE Synthesizer/Mentor Graphics Precision RTL) and then verify the implemented logic with different hardware modules/kits (CPLD/FPGA kits).

• The students are required to acquire the knowledge in both the Platforms (Xilinx and Mentor graphics) by perform at least FIVE experiments on each Platform.

List of Experiments:

1. Realization of Logic gates.
2. Parity Encoder.
3. Random Counter
4. Single Port Synchronous RAM.
5. Synchronous FIFO.
6. ALU.
7. UART Model.
8. Dual Port Asynchronous RAM.
10. Traffic Light Controller using Sequential Logic circuits


12. Finite State Machine (FSM) based logic circuit.

Lab Requirements:

Software:

Xilinx ISE Suite 13.2 Version, Mentor Graphics-Questa Simulator, Mentor Graphics-Precision RTL

Hardware:

Personal Computer with necessary peripherals, configuration and operating System and relevant VLSI (CPLD/FPGA) hardware Kits.