Linear IC Applications

UNIT -1

DIFFERENTIAL AMPLIFIER

OPERATIONAL AMPLIFIER:

The operational amplifier is a direct-coupled high gain amplifier usable from 0 to over 1MH Z to which feedback is added to control its overall response characteristic i.e. gain and bandwidth. The op-amp exhibits the gain down to zero frequency.

Such direct coupled (dc) amplifiers do not use blocking (coupling and by pass) capacitors since these would reduce the amplification to zero at zero frequency. Large by pass capacitors may be used but it is not possible to fabricate large capacitors on a IC chip. The capacitors fabricated are usually less than 20 pf. Transistor, diodes and resistors are also fabricated on the same chip.

DIFFERENTIAL AMPLIFIER:

Differential amplifier is a basic building block of an op-amp. The function of a differential amplifier is to amplify the difference between two input signals.

How the differential amplifier is developed? Let us consider two emitter-biased circuits as shown in fig.1

![Fig. 1](image-url)
The two transistors Q1 and Q2 have identical characteristics. The resistances of the circuits are equal, i.e. $R_{E1} = R_{E2}$, $R_{C1} = R_{C2}$ and the magnitude of $+V_{CC}$ is equal to the magnitude of $-V_{EE}$. These voltages are measured with respect to ground.

To make a differential amplifier, the two circuits are connected as shown in fig. 1. The two $+V_{CC}$ and $-V_{EE}$ supply terminals are made common because they are same. The two emitters are also connected and the parallel combination of $R_{E1}$ and $R_{E2}$ is replaced by a resistance $R_E$. The two input signals $v_1$ & $v_2$ are applied at the base of Q1 and at the base of Q2. The output voltage is taken between two collectors. The collector resistances are equal and therefore denoted by $R_C = R_{C1} = R_{C2}$.

Ideally, the output voltage is zero when the two inputs are equal. When $v_1$ is greater then $v_2$ the output voltage with the polarity shown appears. When $v_1$ is less than $v_2$, the output voltage has the opposite polarity.

The four differential amplifier configurations are following:
1. Dual input, balanced output differential amplifier.
2. Dual input, unbalanced output differential amplifier.
These configurations are shown in fig 2, and are defined by number of input signals used and the way an output voltage is measured. If use two input signals, the configuration is said to be dual input, otherwise it is a single input configuration. On the other hand, if the output voltage is measured between two collectors, it is referred to as a balanced output because both the collectors are at the same dc potential w.r.t. ground. If the output is measured at one of the collectors w.r.t. ground, the configuration is called an unbalanced output.

A multistage amplifier with a desired gain can be obtained using direct connection between successive stages of differential amplifiers. The advantage of direct coupling is that it removes the lower cut off frequency imposed by the coupling capacitors, and they are therefore, capable of amplifying dc as well as ac input signals.

**DUAL INPUT , BALANCED OUTPUT DIFFERENTIAL AMPLIFIER :**
The circuit is shown in fig 1, v1 and v2 are the two inputs, applied to the bases of Q1 and Q2 transistors. The output voltage is measured between the two collectors C1 and C2 , which are at same dc potentials.

**DC ANALYSIS :**
To obtain the operating point (ICC and VCEQ) for differential amplifier dc equivalent circuit is drawn by reducing the input voltages v1 and v2 to zero as shown in fig. 3.
The internal resistances of the input signals are denoted by $R_S$ because $R_{S1} = R_{S2}$. Since both emitter biased sections of the different amplifier are symmetrical in all respects, therefore, the operating point for only one section need to be determined. The same values of $I_{CQ}$ and $V_{CEQ}$ can be used for second transistor $Q_2$.

Applying KVL to the base emitter loop of the transistor $Q_1$.

$$R_S \cdot I_b + V_{BE} + 2I_E \cdot R_E = V_{EE}$$

But $I_b = \frac{I_E}{\beta_{dc}}$ and $I_c \approx I_E$

$$\therefore I_E = I_c = \frac{V_{EE} - V_{BE}}{2R_E + R_S / \beta_{dc}} \quad (E-1)$$

$V_{BE} = 0.6V$ for $S_i$ and 0.2V for $G_e$.

Generally $\frac{R_S}{\beta_{dc}} << 2R_E$ because $R_S$ is the internal resistance of input signal.

$$\therefore I_E = I_c = \frac{V_{EE} - V_{BE}}{2R_E}$$

The value of $R_E$ sets up the emitter current in transistors $Q_1$ and $Q_2$ for a given value of $V_{EE}$. The emitter current in $Q_1$ and $Q_2$ are independent of collector resistance $R_C$.

The voltage at the emitter of $Q_1$ is approximately equal to $-V_{BE}$ if the voltage drop across $R$ is negligible. Knowing the value of $I_C$ the voltage at the collector $V_C$ is given by

$$V_C = V_{CC} - I_c \cdot R_c$$

and $V_{CE} = V_C - V_E$

$$= V_{CC} - I_c \cdot R_C + V_{BE}$$
\[ V_{CE} = V_{CC} + V_{BE} - I_C R_C \quad (E-2) \]

From the two equations VCEQ and ICQ can be determined. This dc analysis applicable for all types of differential amplifier.

**Example - 1**
The following specifications are given for the dual input, balanced-output differential amplifier of fig.1:

\( R_C = 2.2 \text{K ohm}, \, R_B = 4.7 \text{ K ohm}, \, R_{in1} = R_{in2} = 50 \text{ ohm}, \, +V_{CC} = 10 \text{V}, \, -V_{EE} = -10 \text{V}, \, \beta_{dc} = 100 \) and \( V_{BE} = 0.715 \text{V}. \) Determine the operating points (ICQ and VCEQ) of the two transistors.

\[ I_{CQ} = I_E = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_{in}}{\beta_{dc}}} \]

\[ = \frac{10 - 0.715}{9.4 \text{k}\Omega + \frac{50}{100}} = 0.988 \text{mA} \]

\[ V_{CEO} = V_{CE} + V_{BE} - R_C I_{CQ} \]

\[ = 10 + 0.715 - (2.2 \text{k}\Omega)(0.988 \text{mA}) \]

\[ = 8.54 \text{V} \]

The values of ICQ and VCEO are same for both the transistors.

**DIFFERENTIAL INPUT RESISTANCE:**
Differential input resistance is defined as the equivalent resistance that would be measured at either input terminal with the other terminal grounded. This means that the input resistance \( R_{i1} \) seen from the input signal source \( v_1 \) is determined with the signal source \( v_2 \) set at zero. Similarly, the input signal \( v_1 \) is set at zero to determine the input resistance \( R_{i2} \) seen from the input signal source \( v_2 \). Resistance \( R_{S1} \) and \( R_{S2} \) are ignored because they are very small.

\[ R_{i1} = \left. \frac{\beta f_{e}'}{R_E} \right|_{v_2 = 0} \]

\[ = \left. \frac{v_1}{I_e f_{e}'} \right|_{v_2 = 0} = 0 \]

Substituting in eq.1.

\[ R_{i1} = \frac{\beta f_{e}'}{r_e + 2R_E} \]

Since \( R_E >> r_e \)

\[ \Rightarrow r_e + 2R_E >> 2R_E \]

or \( r_e + R_E >> R_E \)

\[ \Rightarrow R_{i1} = 2 \beta f_{e}' \quad (E-3) \]
Similarly,

$$R_{i2} = \left. \frac{V_2}{I_2} \right|_{\beta_1 = 0}$$

$$= \left. \frac{V_2}{I_2 / \beta_{N1}} \right|_{\beta_1 = 0}$$

$$R_{i2} = 2\beta r'_e \quad \text{(E - 4)}$$

The factor of 2 arises because the $r'$ of each transistor is in series.

To get very high input impedance with differential amplifier is to use Darlington transistors. Another way is to use FET.

**OUTPUT RESISTANCE :**

Output resistance is defined as the equivalent resistance that would be measured at output terminal with respect to ground. Therefore, the output resistance $R_{O1}$ measured between collector $C1$ and ground is equal to that of the collector resistance $R_C$. Similarly the output resistance $R_{O2}$ measured at $C2$ with respect to ground is equal to that of the collector resistor $R_C$.

$$R_{O1} = R_{O2} = R_C \quad \text{(E - 5)}$$

The current gain of the differential amplifier is undefined. Like CE amplifier the differential amplifier is a small signal amplifier. It is generally used as a voltage amplifier and not as current or power amplifier.

A dual input, balanced output difference amplifier circuit is shown in fig. 1.
Inverting & Non-Inverting Inputs:

In differential amplifier the output voltage $v_O$ is given by

$$v_O = A_d (v_1 - v_2)$$

When $v_2 = 0$, $v_O = A_d v_1$

When $v_1 = 0$, $v_O = -A_d v_2$

Therefore the input voltage $v_1$ is called the non-inverting input because a positive voltage $v_1$ acting alone produces a positive output voltage $v_O$. Similarly, the positive voltage $v_2$ acting alone produces a negative output voltage hence $v_2$ is called inverting input. Consequently $B_1$ is called non-inverting input terminal and $B_2$ is called inverting input terminal.

**COMMON MODE GAIN:**

A common mode signal is one that drives both inputs of a differential amplifier equally. The common mode signal is interference, static and other kinds of undesirable pickup etc. The connecting wires on the input bases act like small antennas. If a differential amplifier is operating in an environment with lot of electromagnetic interference, each base picks up an unwanted interference voltage. If both the transistors were matched in all respects then the balanced output would be theoretically zero. This is the important characteristic of a differential amplifier. It discriminates against common mode input signals. In other words, it refuses to amplify the common mode signals. The practical effectiveness of rejecting the common signal depends on the degree of matching between the two CE stages forming the differential amplifier. In other words, more closely are the currents in the input transistors, the better is the common mode signal rejection e.g. If $v_1$ and $v_2$ are the two input signals, then the output of a practical op-amp cannot be described by simply

$$v_O = A_d (v_1 - v_2)$$

In practical differential amplifier, the output depends not only on difference signal but also upon the common mode signal (average).

$$v_d = (v_1 - v_d)$$
and \( v_C = \frac{1}{2} (v_1 + v_2) \)

The output voltage, therefore can be expressed as

\[ v_o = A_1 v_1 + A_2 v_2 \]

Where \( A_1 \) & \( A_2 \) are the voltage amplification from input 1(2) to output under the condition that input 2 (1) is grounded.

\[ v_1 = v_C + \frac{1}{2} v_d \quad v_2 = v_C - \frac{1}{2} v_d \]

Substituting \( v_1 \) & \( v_2 \) in output voltage equation

\[ v_o = A_1 (v_C + \frac{1}{2} v_d) + A_2 (v_C - \frac{1}{2} v_d) \]

\[ = \frac{1}{2} (A_1 - A_2) v_d + (A_1 - A_2) v_C \]

\[ = A_d v_d + A_C v_C \]

The voltage gain for the difference signal is \( A_d \) and for the common mode signal is \( A_C \).

The ability of a differential amplifier to reject a common mode signal is expressed by its common mode rejection ratio (CMRR). It is the ratio of differential gain \( A_d \) to the common mode gain \( A_C \).

\[ \text{CMRR} = \frac{A_d}{A_C} = \rho \]

\[ v_o = A_d v_d \left( 1 + \frac{1}{\rho} \frac{V_C}{v_d} \right) \]

Date sheet always specify CMRR in decibels \( \text{CMRR} = 20 \log \text{CMRR} \).

**Dual Input, Unbalanced Output Differential Amplifier:**

In this case, two input signals are given however the output is measured at only one of the two-collector w.r.t. ground as shown in fig. 2. The output is referred to as an unbalanced output because the collector at which the output voltage is measured is at some finite dc potential with respect to ground.
In other words, there is some dc voltage at the output terminal without any input signal applied. DC analysis is exactly same as that of first case.

\[ I_E = I_{CQ} = \frac{V_{EE} - V_{BE}}{2R_E + \frac{R_2}{\beta_{dc}}} \]

\[ V_{CE0} = V_{CC} + V_{BE} - I_{CQ}R_C \]

**AC Analysis:**
The output voltage gain in this case is given by

\[ A_d = \frac{V_o}{V_d} = \frac{R_C}{2r'_e} \]

The voltage gain is half the gain of the dual input, balanced output differential amplifier. Since at the output there is a dc error voltage, therefore, to reduce the voltage to zero, this configuration is normally followed by a level translator circuit.

**Differential amplifier with swamping resistors:**
By using external resistors R'_e in series with each emitter, the dependence of voltage gain on variations of r'_e can be reduced. It also increases the linearity range of the differential amplifier. Fig. 3, shows the differential amplifier with swamping resistor R'_e. The value of R'_e is usually large enough to swamp the effect of r'_e.
Constant Current Bias:

In the dc analysis of differential amplifier, we have seen that the emitter current $I_E$ depends upon the value of $\beta_{dc}$. To make operating point stable $I_E$ current should be constant irrespective value of $\beta_{dc}$. For constant $I_E$, $R_E$ should be very large. This also increases the value of CMRR but if $R_E$ value is increased to very large value, $I_E$ (quiescent operating current) decreases. To maintain
same value of $I_E$, the emitter supply $V_{EE}$ must be increased. To get very high value of resistance $R_E$ and constant $I_E$, current, current bias is used.

Fig. 1 shows the dual input balanced output differential amplifier using a constant current bias. The resistance $R_E$ is replace by constant current transistor Q3. The dc collector current in Q3 is established by $R_1$, $R_2$, & $R_E$.

Applying the voltage divider rule, the voltage at the base of Q3 is

$$V_{b3} = \frac{R_2}{R_1 + R_2} (-V_{EE})$$
$$V_{E3} = V_{b3} - V_{BE3}$$
$$= -\frac{R_2}{R_1 + R_2} V_{EE} - V_{BE3}$$
$$I_{BE3} = I_{C3} = \frac{V_E - (-V_{EE})}{R_E}$$
$$= \frac{V_{EE} - \left(\frac{R_2}{R_1 + R_2}\right) V_{EE} - V_{BE3}}{R_E}$$

Because the two halves of the differential amplifiers are symmetrical, each has half of the current $I_{C3}$.

$$I_{E1} = I_{E2} = \frac{I_{C3}}{2} = \frac{V_{EE} - \left(\frac{R_2}{R_1 + R_2} V_{EE}\right)}{2R_E} - V_{BE3}$$
The collector current, IC3 in transistor Q3 is fixed because no signal is injected into either the emitter or the base of Q3. Besides supplying constant emitter current, the constant current bias also provides a very high source resistance since the ac equivalent or the dc source is ideally an open circuit. Therefore, all the performance equations obtained for differential amplifier using emitter bias are also valid. As seen in IE expressions, the current depends upon VBE3. If temperature changes, VBE changes and current IE also changes. To improve thermal stability, a diode is placed in series with resistance R1 as shown in fig. 2.

![Fig. 2](image)

This helps to hold the current IE3 constant even though the temperature changes. Applying KVL to the base circuit of Q3.

\[
(V_{EE} - V_D) \frac{R_1}{R_1 + R_2} + V_D = V_{BE3} + I_{E3} R_E
\]

where \(V_D\) is the diode voltage. Thus,

\[
I_{E3} = \frac{1}{R_E} \left\{ \frac{V_{EE}}{R_1 + R_2} + V_D - \frac{R_1}{R_1 + R_2} \cdot V_{BE3} \right\}
\]

If \(R_1\) and \(R_2\) are so chosen that

\[
\frac{R_2}{R_1 + R_2} \cdot V_D = V_{BE3}
\]

then,

\[
I_{E3} = \frac{1}{R_3} \cdot \frac{V_{EE} R_1}{R_1 + R_2}
\]
Therefore, the current IE3 is constant and independent of temperature because of the added diode D. Without D the current would vary with temperature because VBE3 decreases approximately by 2mV/° C. The diode has same temperature dependence and hence the two variations cancel each other and IE3 does not vary appreciably with temperature. Since the cut ? in voltage VD of diode approximately the same value as the base to emitter voltage VBE3 of a transistor the above condition cannot be satisfied with one diode. Hence two diodes are used in series for VD. In this case the common mode gain reduces to zero.

Some times zener diode may be used in place of diodes and resistance as shown in fig. 3. Zeners are available over a wide range of voltages and can have matching temperature coefficient. The voltage at the base of transistor Q8 is

\[
V_{B3} = V_Z - V_{EE} \\
V_{E3} = V_{B3} - V_{BE3} \\
\quad = V_Z - V_{EE} - V_{BE3} \\
I_{E3} = \frac{V_{E3} \cdot (V_{EE})}{R_E} \\
\quad = \frac{V_Z - V_{BE3}}{R_E}
\]

The value of R2 is selected so that \(I_2 = 1.2 I_Z\text{(min)}\) where \(I_Z\) is the minimum current required to cause the zener diode to conduct in the reverse region, that is to block the rated voltage \(V_Z\).

\[
R_2 = \frac{V_{EE} \cdot V_Z}{I_2} \\
\text{Where } I_2 = 1.2 I_Z\text{(min)}
\]
UNIT 2
OPERATIONAL AMPLIFIER

1. Objective

The purpose of these experiments is to introduce the most important of all analog building blocks, the operational amplifier (“op-amp” for short). This handout gives an introduction to these amplifiers and a smattering of the various configurations that they can be used in. Apart from their most common use as amplifiers (both inverting and non-inverting), they also find applications as buffers (load isolators), adders, subtractors, integrators, logarithmic amplifiers, impedance converters, filters (low-pass, high-pass, band-pass, band-reject or notch), and differential amplifiers. So let’s get set for a fun-filled adventure with op-amps!

2. Introduction: Amplifier Circuit

Before jumping into op-amps, let’s first go over some amplifier fundamentals.

An amplifier has an input port and an output port. (A port consists of two terminals, one of which is usually connected to the ground node.) In a linear amplifier, the output signal = \( A \times \) input signal, where \( A \) is the amplification factor or “gain.” Depending on the nature of the input and output signals, we can have four types of amplifier gain: voltage gain (voltage out / voltage in), current gain (current out / current in), trans resistance (voltage out / current in) and trans conductance (current out / voltage in). Since most op-amps are used as voltage-to-voltage amplifiers, we will limit the discussion here to this type of amplifier.

The circuit model of an amplifier is shown in Figure 1 (center dashed box, with an input port and an output port). The input port plays a passive role, producing no voltage of its own, and is modeled by a resistive element \( R_i \) called the input resistance. The output port is modeled by a dependent voltage source \( AV_i \) in series with the output resistance \( R_o \), where \( V_i \) is the potential difference between the input port terminals. Figure 1 shows a complete amplifier circuit, which consists of an input voltage source \( V_i \) in series with the source resistance \( R_s \), and an output “load” resistance \( R_L \). From this figure, it can be seen that we have voltage-divider circuits at both the input port and the output port of the amplifier. This requires us to re-calculate \( V_i \) and \( V_o \) whenever a different source and/or load is used:

\[
V_i = \left( \frac{R_i}{R_i + R_s} \right) V_s 
\]  
(1)
Figure 1: Circuit model of an amplifier circuit.

\[ V_o = \left( \frac{R_i}{R_o + R_L} \right) AV_i \]  

(2)

3. The Operational Amplifier: Ideal Op-Amp Model

The amplifier model shown in Figure 1 is redrawn in Figure 2 showing the standard op-amp notation. An op-amp is a “differential-to-single-ended” amplifier, i.e., it amplifies the voltage difference \( V_p - V_n = V_i \) at the input port and produces a voltage \( V_o \) at the output port that is referenced to the ground node of the circuit in which the op-amp is used.

Figure 2: Standard op-amp  

Figure 3: Ideal op-amp

The ideal op-amp model was derived to simplify circuit analysis and it is commonly used by engineers for first-order approximate calculations. The ideal model makes three simplifying assumptions:

Gain is infinite: \( A = \infty \)  

(3)

Input resistance is infinite: \( R_i = \infty \)  

(4)

Output resistance is zero: \( R_o = 0 \)  

(5)
Applying these assumptions to the standard op-amp model results in the ideal op-amp model shown in Figure 3. Because $R_i = \infty$ and the voltage difference $V_p - V_n = V_i$ at the input port is finite, the input currents are zero for an ideal op-amp:

$$i_n = i_p = 0$$  \hspace{1cm} (6)

Hence there is no loading effect at the input port of an ideal op-amp:

$$V_i = V_s$$  \hspace{1cm} (7)

In addition, because $R_o = 0$, there is no loading effect at the output port of an ideal op-amp:

$$V_o = A \times V_i$$  \hspace{1cm} (8)

Finally, because $A = \infty$ and $V_o$ must be finite, $V_i = V_p - V_n = 0$, or

$$V_p = V_n$$  \hspace{1cm} (9)

**Note:** Although Equations 3-5 constitute the ideal op-amp assumptions, Equations 6 and 9 are used most often in solving op-amp circuits.

**Figure 4a:** Non-inverting amplifier  \hspace{1cm} **Figure 5a:** Voltage follower  \hspace{1cm} **Figure 6a:** Inverting amplifier

In addition, because $R_o = 0$, there is no loading effect at the output port of an ideal op-amp:
4. Non-Inverting Amplifier

An ideal op-amp by itself is not a very useful device, since any finite non-zero input signal would result in infinite output. (For a real op-amp, the range of the output signal amplitudes is limited by the positive and negative power-supply voltages – referred to as “the rails”.) However, by connecting external components to the ideal op-amp, we can construct useful amplifier circuits.

Figure 4a shows a basic op-amp circuit, the non-inverting amplifier. The triangular block symbol is used to represent an ideal op-amp. The input terminal marked with a “+” (corresponding to \( V_p \)) is called the non-inverting input; the input terminal marked with a “−” (corresponding to \( V_n \)) is called the inverting input.
To understand how the non-inverting amplifier circuit works, we need to derive a relationship between the input voltage \( V_{in} \) and the output voltage \( V_{out} \). For an ideal op-amp, there is no loading effect at the input, so

\[
V_p = V_i \quad (10)
\]

Since the current flowing into the inverting input of an ideal op-amp is zero, the current flowing through \( R_1 \) is equal to the current flowing through \( R_2 \) (by Kirchhoff’s Current Law -- which states that the algebraic sum of currents flowing into a node is zero -- to the inverting input node). We can therefore apply the voltage-divider formula find \( V_n \):

\[
V_n = \left( \frac{R_1}{R_1 + R_2} \right) V_{out} \quad (11)
\]

From Equation 9, we know that \( V_{in} = V_p = V_n \), so

\[
V_{out} = \left( 1 + \frac{R_2}{R_1} \right) V_{in} \quad (12)
\]

The voltage transfer curve (\( V_{out} \) vs. \( V_{in} \)) for a non-inverting amplifier is shown in Figure 4b. Notice that the gain \( (V_{out} / V_{in}) \) is always greater than or equal to one.

The special op-amp circuit configuration shown in Figure 5a has a gain of unity, and is called a “voltage follower.” This can be derived from the non-inverting amplifier by letting \( R_1 = \infty \) and \( R_2 = 0 \) in Equation 12. The voltage transfer curve is shown in Figure 5b. A frequently asked question is why the voltage follower is useful, since it just copies input signal to the output. The reason is that it isolates the signal source and the load. We know that a signal source usually has an internal series resistance (\( R_s \) in Figure 1, for example). When it is directly connected to a load, especially a heavy (high conductance) load, the output voltage across the load will degrade (according to the voltage-divider formula). With a voltage-follower circuit placed between the source and the load, the signal source sees a light (low conductance) load -- the input resistance of the op-amp. At the same time, the load is driven by a powerful driving source -- the output of the op-amp.

5. Inverting Amplifier

Figure 6a shows another useful basic op-amp circuit, the inverting amplifier. It is similar to the non-inverting circuit shown in Figure 4a except that the input signal is applied to the inverting terminal via \( R_1 \) and the non-inverting terminal is grounded. Let’s derive a relationship between the input voltage \( V_{in} \) and the output voltage \( V_{out} \). First, since \( V_n = V_p \) and \( V_p \) is grounded, \( V_n = 0 \). Since the current flowing into the inverting input of an ideal op-amp is zero, the current flowing through \( R_1 \) must be equal in magnitude and opposite in direction to the current flowing through \( R_2 \) (by Kirchhoff’s Current Law):

\[
V_{out} = \left( 1 + \frac{R_2}{R_1} \right) V_{in} \quad (12)
\]
\[
\frac{V_{in} - V_n}{R_1} = \frac{V_{out} - V_n}{R_2}
\]

(13)

Since \(V_n = 0\), we have:

\[
V_{out} = \left(-\frac{R_2}{R_1}\right)V_{in}
\]

(14)

The gain of inverting amplifier is always negative, as shown in Figure 6b.

6. Operation Circuit

Figure 7 shows an operation circuit, which combines the non-inverting and inverting amplifier. Let’s derive the relationship between the input voltages and the output voltage \(V_{out}\). We can start with the non-inverting input node. Applying Kirchhoff’s Current Law, we obtain:

\[
\frac{V_{B1} - V_p}{R_{B1}} + \frac{V_{B2} - V_p}{R_{B2}} + \frac{V_{B3} - V_p}{R_{B3}} = \frac{V_p}{R_B}
\]

(15)

Applying Kirchhoff’s Current Law to the inverting input node, we obtain:

\[
\frac{V_{A1} - V_n}{R_{A1}} + \frac{V_{A2} - V_n}{R_{A2}} + \frac{V_{A3} - V_n}{R_{A3}} = \frac{V_n - V_{out}}{R_A}
\]

(16)

Since \(V_n = V_p\) (from Equation 9), we can combine Equations 15 and 16 to get

\[
V_{out}\left(\frac{R_{A'}}{R_A}\right) = \left(\frac{V_{B1}}{R_{B1}} + \frac{V_{B2}}{R_{B2}} + \frac{V_{B3}}{R_{B3}}\right)R_{B'} - \left(\frac{V_{A1}}{R_{A1}} + \frac{V_{A2}}{R_{A2}} + \frac{V_{A3}}{R_{A3}}\right)R_{A'}
\]

(17)

where

\[
R_{A'} = \frac{1}{\frac{1}{R_A} + \frac{1}{R_{A1}} + \frac{1}{R_{A2}} + \frac{1}{R_{A3}}}
\]

and

\[
R_{B'} = \frac{1}{\frac{1}{R_B} + \frac{1}{R_{B1}} + \frac{1}{R_{B2}} + \frac{1}{R_{B3}}}
\]
Thus, this circuit adds $V_{B1}$, $V_{B2}$ and $V_{B3}$ and subtracts $V_{A1}$, $V_{A2}$ and $V_{A3}$. Different coefficients can be applied to the input signals by adjusting the resistors. If all the resistors have the same value, then

$$V_{\text{out}} = \left( V_{B1} + V_{B2} + V_{B3} \right) - \left( V_{A1} + V_{A2} + V_{A3} \right)$$

(18)

Figure 7: Operation circuit

7. Integrator

By adding a capacitor in parallel with the feedback resistor $R_2$ in an inverting amplifier as shown in Figure 8, the op-amp can be used to perform integration. An ideal or lossless integrator ($R_2 = \infty$) performs the computation $V_{\text{out}} = -\frac{1}{R_1 C} \int V_{\text{in}} \, dt$. Thus, a square-wave input would cause a triangle-wave output. However, in a real circuit ($R_2 < \infty$) there is some decay in the system state at a rate proportional to the state itself. This leads to exponential decay with a time constant of $\tau = R_2 C$.

Figure 8: Integrator

8. Differentiator

By adding a capacitor in series with the input resistor $R_1$ in an inverting amplifier, the op-amp can be used to perform differentiation. An ideal differentiator ($R_1 = 0$) has no memory and performs
the computation \( V_{out} = -R_2 C \frac{dV_{in}}{dt} \). Thus a triangle-wave input would cause a square-wave output. However, a real circuit \((R_1 > 0)\) will have some memory of the system state (like an lossy integrator) with exponential decay of time constant \( \tau = R_1 C \).

9. Differential Amplifier
Figure 9 shows the differential amplifier circuit. As the name suggests, this op-amp configuration amplifies the difference of two input signals.

\[
V_{out} = (V_+ - V_-) \frac{R_2}{R_1} \tag{20}
\]

If the two input signals are the same, the output should be zero, ideally. To quantify the quality of the amplifier, the term Common Mode Rejection Ratio (CMRR) is defined. It is the ratio of the output voltage corresponding to the difference of the two input signals to the output voltage corresponding to “common part” of the two signals. A good op-amp has a high CMRR.

![Figure 9: Differential amplifier](image)

10. Frequency Response of Op-Amp
The “frequency response” of any circuit is the magnitude of the gain in decibels (dB) as a function of the frequency of the input signal. The decibel is a common unit of measurement for the relative loudness of a sound or, in electronics, for the relative magnitude of two power levels. The expression for such a ratio of power is

\[
\text{Power level in dB} = 10 \log_{10} \left( \frac{P_1}{P_2} \right)
\]

(A decibel is one-tenth of a "Bel", a seldom-used unit named for Alexander Graham Bell, inventor of the telephone.) The voltage or current gain of an amplifier expressed in dB is 20 \( \log_{10}|G| \), where \( G = \frac{V_{out}}{V_{in}} \) for voltage gain or \( I_{out}/I_{in} \) for current gain. The frequency response of an op-amp has a low-pass characteristic (passing low-frequency signals, attenuating high-frequency signals), Figure 10.
Figure 10: Frequency response of op-amp.

The bandwidth is the frequency at which the power of the output signal is reduced to half that of the maximum output power. This occurs when the power gain $G$ drops by 3 dB. In Figure 10, the bandwidth is $B$ Hz. For all op-amps, the Gain*Bandwidth product is a constant. Hence, if the gain of an op-amp is decreased, its operational bandwidth increases proportionally. This is an important trade-off consideration in op-amp circuit design. In Sections 3 through 8 above, we assumed that the op-amp has infinite bandwidth.

10. More on Op-Amps
All of the above op-amp configurations have one thing in common: there exists a path from the output of the op-amp back to its inverting input. When the output is not “railed” to a supply voltage, negative feedback ensures that the op-amp operates in the linear region (as opposed to the saturation region, where the output voltage is “saturated” at one of the supply voltages). Amplification, addition/subtraction, and integration/differentiation are all linear operations. Note that both AC signals and DC offsets are included in these operations, unless we add a capacitor in series with the input signal(s) to block the DC component.
An inverting amplifier inverts and scales the input signal. As long as the op-amp gain is very large, the amplifier gain is determined by two stable external resistors (the feedback resistor $R_f$ and the input resistor $R_{in}$) and not by op-amp parameters which are highly temperature dependent. In particular, the $R_{in}-R_f$ resistor network acts as an electronic seesaw (i.e., a class-1 lever) where the inverting (i.e., $-$) input of the operational amplifier is like a fulcrum about which the seesaw pivots. That is, because the operational amplifier is in a negative-feedback configuration, its internal high gain effectively fixes the inverting (i.e., $-$) input at the same 0 V (ground) voltage of the non-inverting (i.e., $+$) input, which is similar to the stiff mechanical support provided by the fulcrum of the seesaw. Continuing the analogy,

Just as the movement of one end of the seesaw is opposite the movement of the other end of the seesaw, positive movement away from 0 V at the input of the $R_{in}-R_f$ network is matched by negative movement away from 0 V at the output of the network; thus, the amplifier is said to be inverting.

In the seesaw analogy, the mechanical moment or torque from the force on one side of the fulcrum is balanced exactly by the force on the other side of the fulcrum; consequently, asymmetric lengths in the seesaw allow for small forces on one side of the seesaw to generate large forces on the other side of the seesaw. In the inverting amplifier, electrical current, like torque, is conserved across the $R_{in}-R_f$ network and relative differences between the $R_{in}$ and $R_f$ resistors allow small voltages on one side of the network to generate large voltages (with opposite sign) on the other side of the network. Thus, the device amplifies (and inverts) the input voltage. However, in this analogy, it is the reciprocals of the resistances (i.e., the conductances or admittances) that play the role of lengths in the seesaw.

Hence, the amplifier output is related to the input as in

$$V_{out} = -\frac{R_f}{R_{in}} V_{in}.$$  

So the voltage gain of the amplifier is $A = -\frac{R_f}{R_{in}}$ where the negative sign is a convention indicating that the output is negated. For example, if $R_f$ is 10 kΩ and $R_{in}$ is 1 kΩ, then the gain is $-10$ kΩ/1 kΩ, or $-10$ (or $-10$ V/V). Moreover, the input impedance of the device is $\frac{R_{in}}{R_f}$ because the operational amplifier's inverting (i.e., $-$) input is a virtual ground.
In a real operational amplifier, the current into its two inputs is small but non-zero (e.g., due to input bias currents). The current into the inverting (i.e., $-$) input of the operational amplifier is drawn across the $R_{in}$ and $R_I$ resistors in parallel, which appears like a small parasitic voltage difference between the inverting (i.e., $-$) and non-inverting (i.e., $+$) inputs of the operational amplifier. To mitigate this practical problem, a third resistor of value $\frac{R_I R_{in}}{R_I + R_{in}}$ can be added between the non-inverting (i.e., $+$) input and the true ground. This resistor does not affect the idealized operation of the device because no current enters the ideal non-inverting input. However, in the practical case, if input currents are roughly equivalent, the voltage added at the inverting input will match the voltage at the non-inverting input, and so this common-mode signal will be ignored by the operational amplifier (which operates on differences between its inputs).

**NON INVERTING AMPLIFIER**

Amplifies a voltage (multiplies by a constant greater than 1)

$$V_{out} = V_{in} \left(1 + \frac{R_2}{R_1}\right)$$

Input impedance $Z_{in} \approx \infty$

The input impedance is *at least* the impedance between non-inverting (†) and inverting (⊥) inputs, which is typically 1 MΩ to 10 TΩ, plus the impedance of the path from the inverting (⊥) input to ground (i.e., $R_I$ in parallel with $R_2$).

Because negative feedback ensures that the non-inverting and inverting inputs match, the input impedance is actually much higher. [dubious – discuss]

Although this circuit has a large input impedance, it suffers from error of input bias current.

The non-inverting (†) and inverting (⊥) inputs draw small leakage currents into the operational amplifier.

These input currents generate voltages that act like unmodeled input offsets. These unmodeled effects can lead to noise on the output (e.g., offsets or drift).
Assuming that the two leaking currents are matched, their effect can be mitigated by ensuring the DC impedance looking out of each input is the same.

The voltage produced by each bias current is equal to the product of the bias current with the equivalent DC impedance looking out of each input. Making those impedances equal makes the offset voltage at each input equal, and so the non-zero bias currents will have no impact on the difference between the two inputs.

A resistor of value

\[ R_{1||2} = \left( \frac{1}{R_1} + \frac{1}{R_2} \right)^{-1} = \frac{R_1R_2}{R_1 + R_2}, \]

which is the equivalent resistance of \( R_1 \) in parallel with \( R_2 \), between the \( V_{\text{in}} \) source and the non-inverting (\(+\)) input will ensure the impedances looking out of each input will be matched.

The matched bias currents will then generate matched offset voltages, and their effect will be hidden to the operational amplifier (which acts on the difference between its inputs) so long as the CMRR is good.

Very often, the input currents are not matched.

Most operational amplifiers provide some method of balancing the two input currents (e.g., by way of an external potentiometer).

Alternatively, an external offset can be added to the operational amplifier input to nullify the effect.

Another solution is to insert a variable resistor between the \( V_{\text{in}} \) source and the non-inverting (\(+\)) input. The resistance can be tuned until the offset voltages at each input are matched.

Operational amplifiers with MOSFET-based input stages have input currents that are so small that they often can be neglected.

**VOLTAGE AMPLIFIER**

Used as a buffer amplifier to eliminate loading effects (e.g., connecting a device with a high source impedance to a device with a low input impedance).

\[
\begin{align*}
V_{\text{out}} &= V_{\text{in}} \\
Z_{\text{in}} &= \infty \quad (\text{realistically, the differential input impedance of the op-amp itself, 1 MΩ to 1 TΩ})
\end{align*}
\]

Due to the strong (i.e., unity gain) feedback and certain non-ideal characteristics of real operational amplifiers, this feedback system is prone to have poor stability margins.
Consequently, the system may be unstable when connected to sufficiently capacitive loads. In these cases, a lag compensation network (e.g., connecting the load to the voltage follower through a resistor) can be used to restore stability. The manufacturer data sheet for the operational amplifier may provide guidance for the selection of components in external compensation networks. Alternatively, another operational amplifier can be chosen that has more appropriate internal compensation.

**INSTRUMENTATION AMPLIFIER**

Combines very high input impedance, high common-mode rejection, low DC offset, and other properties used in making very accurate, low-noise measurements

Is made by adding a non-inverting buffer to each input of the differential amplifier to increase the input impedance.
UNIT 4
NON LINEAR APPLICATIONS OF OPAMP

SCHMITT TRIGGER
A bistable multivibrator implemented as a comparator with hysteresis.

In this configuration, the input voltage is applied through the resistor \( R_1 \) (which may be the source internal resistance) to the non-inverting input and the inverting input is grounded or referenced. The hysteresis curve is non-inverting and the switching thresholds are

\[
\pm \frac{R_1}{R_2} V_{sat}
\]

where \( V_{sat} \) is the greatest output magnitude of the operational amplifier.

PRECISION RECTIFIER

The voltage drop \( V_F \) across the forward biased diode in the circuit of a passive rectifier is undesired. In this active version, the problem is solved by connecting the diode in the
negative feedback loop. The op-amp compares the output voltage across the load with the
input voltage and increases its own output voltage with the value of $V_F$. As a result, the
voltage drop $V_F$ is compensated and the circuit behaves very nearly as an ideal
(super) diode with $V_F = 0 \text{ V}$.

The circuit has speed limitations at high frequency because of the slow negative feedback and
due to the low slew rate of many non-ideal op-amps.

LOGARITHMIC OUTPUT

The relationship between the input voltage $v_{\text{in}}$ and the output voltage $v_{\text{out}}$ is given by:

$$v_{\text{out}} = -V_T \ln \left( \frac{v_{\text{in}}}{I_S R} \right)$$

where $I_S$ is the saturation current and $V_T$ is the thermal voltage.

If the operational amplifier is considered ideal, the negative pin is virtually grounded, so the
current flowing into the resistor from the source (and thus through the diode to the output, since
the op-amp inputs draw no current) is:

$$\frac{v_{\text{in}}}{R} = I_R = I_D$$

where $I_D$ is the current through the diode. As known, the relationship between the current and
the voltage for a diode is:

$$I_D = I_S \left( e^{\frac{v_{\text{in}}}{K T}} - 1 \right).$$

This, when the voltage is greater than zero, can be approximated by:

$$I_D \approx I_S e^{\frac{v_{\text{in}}}{K T}}.$$

Putting these two formulae together and considering that the output voltage is the negative of the
voltage across the diode ($V_{\text{out}} = -V_D$), the relationship is proven.

This implementation does not consider temperature stability and other non-ideal effects.
EXPONENTIAL OUTPUT

The relationship between the input voltage $V_{in}$ and the output voltage $V_{out}$ is given by:

$$V_{out} = -RI_S e^{\frac{V_in}{V_T}}$$

where $I_S$ is the saturation current and $V_T$ is the thermal voltage.

Considering the operational amplifier ideal, then the negative pin is virtually grounded, so the current through the diode is given by:

$$I_D = I_S \left( e^{\frac{V_{in}}{V_T}} - 1 \right)$$

when the voltage is greater than zero, it can be approximated by:

$$I_D \approx I_S e^{\frac{V_{in}}{V_T}}.$$

The output voltage is given by:

$$V_{out} = -RI_D.$$
An active filter is a type of analog electronic filter that uses active components such as an amplifier. Amplifiers included in a filter design can be used to improve the performance and predictability of a filter, while avoiding the need for inductors (which are typically expensive compared to other components). An amplifier prevents the load impedance of the following stage from affecting the characteristics of the filter. An active filter can have complex poles and zeros without using a bulky or expensive inductor. The shape of the response, the Q (quality factor), and the tuned frequency can often be set with inexpensive variable resistors. In some active filter circuits, one parameter can be adjusted without affecting the others.

Using active elements has some limitations. Basic filter design equations neglect the finite bandwidth of amplifiers. Available active devices have limited bandwidth, so they are often impractical at high frequencies. Amplifiers consume power and inject noise into a system. Certain circuit topologies may be impractical if no DC path is provided for bias current to the amplifier elements. Power handling capability is limited by the amplifier stages.

What is a filter?
A filter is a device that passes electric signals at certain frequencies or frequency ranges while preventing the passage of others. — Webster.

Filter circuits are used in a wide variety of applications. In the field of telecommunication, band-pass filters are used in the audio frequency range (0 kHz to 20 kHz) for modems and speech processing. High-frequency band-pass filters (several hundred MHz) are used for channel selection in telephone central offices. Data acquisition systems usually require anti-aliasing low-pass filters as well as low-pass noise filters in their preceding signal conditioning stages. System power supplies often use band-rejection filters to suppress the 60-Hz line frequency and high frequency transients.

In addition, there are filters that do not filter any frequencies of a complex input signal, but just add a linear phase shift to each frequency component, thus contributing to a constant time
Delay. These are called all-pass filters. At high frequencies (> 1 MHz), all of these filters usually consist of passive components such as inductors (L), resistors (R), and capacitors (C). They are then called LRC filters. In the lower frequency range (1 Hz to 1 MHz), however, the inductor value becomes very large and the inductor itself gets quite bulky, making economical production difficult. In these cases, active filters become important.

Active filters are circuits that use an operational amplifier (op amp) as the active device in combination with some resistors and capacitors to provide an LRC-like filter performance at low frequencies.

Active filters can implement the same transfer functions as passive filters. Common transfer functions are:

- High-pass filter – attenuation of frequencies below their cut-off points.
- Low-pass filter – attenuation of frequencies above their cut-off points.
- Band-pass filter – attenuation of frequencies both above and below those they allow to pass.
- Notch filter – attenuation of certain frequencies while allowing all others to pass.

**HIGH PASS FILTER:**

A **high-pass filter** (HPF) is an electronic filter that passes high-frequency signals but attenuates (reduces the amplitude of) signals with frequencies lower than the cutoff frequency. The actual amount of attenuation for each frequency varies from filter to filter. A high-pass filter is usually modeled as a linear time-invariant system. It is sometimes called a **low-cut filter** or **bass-cut filter**. High-pass filters have many uses, such as blocking DC from circuitry sensitive to non-zero average voltages or RF devices. They can also be used in conjunction with a low-pass filter to make a bandpass filter.

![High-pass filter diagram](image)

A passive, analog, first-order high-pass filter, realized by an RC circuit
LOW PASS FILTER:

A low-pass filter is a filter that passes low-frequency signals and attenuates (reduces the amplitude of) signals with frequencies higher than the cutoff frequency. The actual amount of attenuation for each frequency varies depending on specific filter design. It is sometimes called a high-cut filter, or treble cut filter in audio applications. A low-pass filter is the opposite of a high-pass filter. A band-pass filter is a combination of a low-pass and a high-pass.

Low-pass filters exist in many different forms, including electronic circuits (such as a *hiss filter* used in audio), anti-aliasing filters for conditioning signals prior to analog-to-digital conversion, digital filters for smoothing sets of data, acoustic barriers, blurring of images, and so on. The moving average operation used in fields such as finance is a particular kind of low-pass filter, and can be analyzed with the same signal processing techniques as are used for other low-pass filters. Low-pass filters provide a smoother form of a signal, removing the short-term fluctuations, and leaving the longer-term trend.

An optical filter can correctly be called a low-pass filter, but conventionally is called a *longpass* filter (low frequency is long wavelength), to avoid confusion.
A simple low-pass RC filter

![A simple low-pass RC filter diagram](image)

An active low-pass filter

**BAND PASS FILTER:**

A band-pass filter is a device that passes frequencies within a certain range and rejects (attenuates) frequencies outside that range.

Optical band-pass filters are of common usage.

An example of an analogue electronic band-pass filter is an RLC circuit (a resistor–inductor–capacitor circuit). These filters can also be created by combining a low-pass filter with a high-pass filter.

*Bandpass* is an adjective that describes a type of filter or filtering process; it is to be distinguished from passband, which refers to the actual portion of affected spectrum. Hence, one might say "A dual bandpass filter has two passbands." A *bandpass signal* is a signal containing a band of frequencies away from zero frequency, such as a signal that comes out of a bandpass filter.
A band-pass filter.

Bandwidth measured at half-power points (gain -3 dB, \(\sqrt{2}/2\), or about 0.707 relative to peak) on a diagram showing magnitude transfer function versus frequency for a band-pass filter.

An ideal bandpass filter would have a completely flat passband (e.g., with no gain/attenuation throughout) and would completely attenuate all frequencies outside the passband. Additionally, the transition out of the passband would be instantaneous in frequency. In practice, no bandpass filter is ideal. The filter does not attenuate all frequencies outside the desired frequency range completely; in particular, there is a region just outside the intended passband where frequencies are attenuated, but not rejected. This is known as the filter roll-off, and it is usually expressed in dB of attenuation per octave or decade of frequency. Generally, the design of a filter seeks to make the roll-off as narrow as possible, thus allowing the filter to perform as close as possible to its intended design. Often, this is achieved at the expense of pass-band or stop-band ripple.

The bandwidth of the filter is simply the difference between the upper and lower cutoff frequencies. The shape factor is the ratio of bandwidths measured using two different attenuation values to determine the cutoff frequency, e.g., a shape factor of 2:1 at 30/3 dB means the bandwidth measured between frequencies at 30 dB attenuation is twice that measured between frequencies at 3 dB attenuation.

Outside of electronics and signal processing, one example of the use of band-pass filters is in the atmospheric sciences. It is common to band-pass filter recent meteorological data with a period range of, for example, 3 to 10 days, so that only cyclones remain as fluctuations in the data fields.
**BAND STOP FILTER:**

In signal processing, a band-stop filter or band-rejection filter is a filter that passes most frequencies unaltered, but attenuates those in a specific range to very low levels. It is the opposite of a band-pass filter. A notch filter is a band-stop filter with a narrow stopband (high Q factor).

Narrow notch filters (optical) are used in Raman spectroscopy, live sound reproduction (public address systems, or PA systems) and in instrument amplifiers (especially amplifiers or preamplifiers for acoustic instruments such as acoustic guitar, mandolin, bass instrument amplifier, etc.) to reduce or prevent audio feedback, while having little noticeable effect on the rest of the frequency spectrum (electronic or software filters). Other names include 'band limit filter', 'T-notch filter', 'band-elimination filter', and 'band-reject filter'.

Typically, the width of the stopband is 1 to 2 decades (that is, the highest frequency attenuated is 10 to 100 times the lowest frequency attenuated). However, in the audio band, a notch filter has high and low frequencies that may be only semitones apart.

![Generic electrical schematic of a simple band-stop filter](image-url)
A generic ideal band-stop filter, showing both positive and negative angular frequencies
Unit 6

TIMER

The 555 timer IC is an integrated circuit (chip) used in a variety of timer, pulse generation, and oscillator applications. The 555 can be used to provide time delays, as an oscillator, and as a flip-flop element. Derivatives provide up to four timing circuits in one package.

Introduced in 1971 by Signetics, the 555 is still in widespread use due to its ease of use, low price, and good stability. It is now made by many companies in the original bipolar and also in low-power CMOS types. As of 2003, it was estimated that 1 billion units are manufactured every year.

The IC was designed in 1971 by Hans Camenzind under contract to Signetics, which was later acquired by Philips (now NXP).

Depending on the manufacturer, the standard 555 package includes 25 transistors, 2 diodes and 15 resistors on a silicon chip installed in an 8-pin mini dual-in-line package (DIP-8). Variants available include the 556 (a 14-pin DIP combining two 555s on one chip), and the two 558 & 559s (both a 16-pin DIP combining four slightly modified 555s with DIS & THR connected internally, and TR is falling edge sensitive instead of level sensitive).

The NE555 parts were commercial temperature range, 0 °C to +70 °C, and the SE555 part number designated the military temperature range, −55 °C to +125 °C. These were available in both high-reliability metal can (T package) and inexpensive epoxy plastic (V package) packages. Thus the full part numbers were NE555V, NE555T, SE555V, and SE555T. It has been hypothesized that the 555 got its name from the three 5 kΩ resistors used within, but Hans Camenzind has stated that the number was arbitrary.

Low-power versions of the 555 are also available, such as the 7555 and CMOS TLC555. The 7555 is designed to cause less supply noise than the classic 555 and the manufacturer claims that it usually does not require a "control" capacitor and in many cases does not require a decoupling capacitor on the power supply. Such a practice should nevertheless be avoided, because noise produced by the timer or variation in power supply voltage might interfere with other parts of a circuit or influence its threshold voltages.
NE555 from Signetics in dual-in-line package

Internal block diagram

Pinout diagram
The connection of the pins for a DIP package is as follows:

<table>
<thead>
<tr>
<th>Pin</th>
<th>Name</th>
<th>Purpose</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>GND</td>
<td>Ground reference voltage, low level (0 V)</td>
</tr>
<tr>
<td>2</td>
<td>TRIG</td>
<td>The OUT pin goes high and a timing interval starts when this input falls below 1/2 of CTRL voltage (which is typically 2/3 of $V_{CC}$, when CTRL is open).</td>
</tr>
<tr>
<td>3</td>
<td>OUT</td>
<td>This output is driven to approximately 1.7V below $+V_{CC}$ or GND.</td>
</tr>
<tr>
<td>4</td>
<td>RESET</td>
<td>A timing interval may be reset by driving this input to GND, but the timing does not begin again until RESET rises above approximately 0.7 volts. Overrides TRIG which overrides THR.</td>
</tr>
<tr>
<td>5</td>
<td>CTRL</td>
<td>Provides &quot;control&quot; access to the internal voltage divider (by default, 2/3 $V_{CC}$).</td>
</tr>
<tr>
<td>6</td>
<td>THR</td>
<td>The timing (OUT high) interval ends when the voltage at THR is greater than that at CTRL (2/3 $V_{CC}$ if CTRL is open).</td>
</tr>
<tr>
<td>7</td>
<td>DIS</td>
<td>Open collector output which may discharge a capacitor between intervals. In phase with output.</td>
</tr>
<tr>
<td>8</td>
<td>$V_{CC}$</td>
<td>Positive supply voltage, which is usually between 3 and 15 V depending on the variation.</td>
</tr>
</tbody>
</table>

Pin 5 is also sometimes called the CONTROL VOLTAGE pin. By applying a voltage to the CONTROL VOLTAGE input one can alter the timing characteristics of the device. In most applications, the CONTROL VOLTAGE input is not used. It is usual to connect a 10 nF capacitor between pin 5 and 0 V to prevent interference. The CONTROL VOLTAGE input can be used to build an astable with a frequency modulated output.

**Modes**

The 555 has three operating modes:

- **Monostable mode:** In this mode, the 555 functions as a "one-shot" pulse generator. Applications include timers, missing pulse detection, bouncefree switches, touch switches, frequency divider, capacitance measurement, pulse-width modulation (PWM) and so on.
- **Astable (free-running) mode:** The 555 can operate as an oscillator. Uses include LED and lamp flashers, pulse generation, logic clocks, tone generation, security alarms, pulse position modulation and so on. The 555 can be used as a simple ADC, converting an analog value to a pulse length. E.g. selecting a thermistor as timing resistor allows the use of the 555 in a temperature sensor: the period of the output pulse is determined by the temperature. The use of a microprocessor based circuit can then convert the pulse period to temperature, linearize it and even provide calibration means.
Bistable mode or Schmitt trigger: The 555 can operate as a flip-flop, if the DIS pin is not connected and no capacitor is used. Uses include bounce-free latched switches.

Monostable

![Schematic of a 555 in monostable mode](image)

The relationships of the trigger signal, the voltage on C and the pulse width in monostable mode

In the monostable mode, the 555 timer acts as a "one-shot" pulse generator. The pulse begins when the 555 timer receives a signal at the trigger input that falls below a third of the voltage supply. The width of the output pulse is determined by the time constant of an RC network, which consists of a capacitor (C) and a resistor (R). The output pulse ends when the voltage on the capacitor equals 2/3 of the supply voltage. The output pulse width can be lengthened or shortened to the need of the specific application by adjusting the values of R and C.

The output pulse width of time \( t \), which is the time it takes to charge C to 2/3 of the supply voltage, is given by

\[
t = RC \ln(3) \approx 1.1RC
\]
where \( t \) is in seconds, \( R \) is in ohms and \( C \) is in farads.

While using the timer IC in monostable mode, the main disadvantage is that the time span between any two triggering pulses must be greater than the RC time constant.

**Bistable**

![Schematic of a 555 in bistable mode](image)

In bistable mode, the 555 timer acts as a basic flip-flop. The trigger and reset inputs (pins 2 and 4 respectively on a 555) are held high via Pull-up resistors while the threshold input (pin 6) is simply grounded. Thus configured, pulling the trigger momentarily to ground acts as a 'set' and transitions the output pin (pin 3) to Vcc (high state). Pulling the reset input to ground acts as a 'reset' and transitions the output pin to ground (low state). No capacitors are required in a bistable configuration. Pin 5 (control) is connected to ground via a small-value capacitor (usually 0.01 to 0.1 uF); pin 7 (discharge) is left floating.

**Astable**

![Standard 555 astable circuit](image)

In astable mode, the 555 timer puts out a continuous stream of rectangular pulses having a specified frequency. Resistor \( R_1 \) is connected between \( V_{CC} \) and the discharge pin (pin 7) and
another resistor (R2) is connected between the discharge pin (pin 7), and the trigger (pin 2) and threshold (pin 6) pins that share a common node. Hence the capacitor is charged through R1 and R2, and discharged only through R2, since pin 7 has low impedance to ground during output low intervals of the cycle, therefore discharging the capacitor.

In the astable mode, the frequency of the pulse stream depends on the values of R1, R2 and C:

\[ f = \frac{1}{\ln(2) \cdot C \cdot (R1 + 2R2)} \] \[ \text{[7]} \]

The high time from each pulse is given by:

\[ \text{high} = \ln(2) \cdot (R1 + R2) \cdot C \]

and the low time from each pulse is given by:

\[ \text{low} = \ln(2) \cdot R2 \cdot C \]

where R1 and R2 are the values of the resistors in ohms and C is the value of the capacitor in farads.

\[
\frac{V_{cc}^2}{2} \geq \frac{V_{pp}^2}{R2}. 
\]

The power capability of R1 must be greater than \( \frac{V_{pp}^2}{R2} \).

Particularly with bipolar 555s, low values of R1 must be avoided so that the output stays saturated near zero volts during discharge, as assumed by the above equation. Otherwise the output low time will be greater than calculated above. It should be noted that the first cycle will take appreciably longer than the calculated time, as the capacitor must charge from 0V to 2/3 of \( V_{cc} \) from power-up, but only from 1/3 of \( V_{cc} \) to 2/3 of \( V_{cc} \) on subsequent cycles.

The circuit configuration above does not permit a duty cycle of less than 50%, because the time-constant for charging C1 is always greater than for discharging. To achieve any arbitrary duty cycle, R2 can be moved to be in series with pin 7, the discharge pin. The duration of the high-output interval (during the charging of C1) is then 0.693(R1C1), and the low-output interval (while discharging C1) is 0.693(R2C1). The total time period, T, is 0.693(R1+R2)C1. \[ \text{[8]} \]

A more complicated method to achieve a duty cycle of less than 50% is to use a small diode (that is fast enough for the application) in parallel with R2 (instead of placing it on pin 7), with the cathode on the capacitor side. This bypasses R2 during the high part of the cycle so that the high interval depends approximately only on R1 and C. The presence of the diode is a voltage drop that slows charging on the capacitor so that the high time is longer than the expected and often-cited \( \ln(2) \cdot R1 \cdot C = 0.693 \cdot R1 \cdot C \). The low time will be the same as without the diode as shown above. With a diode, the high time is
where $V_{\text{diode}}$ is when the diode has a current of $1/2$ of $V_{\text{cc}}/R_1$ which can be determined from its datasheet or by testing. As an extreme example, when $V_{\text{cc}}=5$ and $V_{\text{diode}}=0.7$, high time $=1.00 \, R_1 \cdot C$ which is 45% longer than the "expected" 0.693 $R_1 \cdot C$. At the other extreme, when $V_{\text{cc}}=15$ and $V_{\text{diode}}=0.3$, the high time $=0.725 \, R_1 \cdot C$ which is closer to the expected 0.693 $R_1 \cdot C$. The equation reduces to the expected 0.693 $R_1 \cdot C$ if $V_{\text{diode}}=0$.

The operation of RESET in this mode is not well defined, some manufacturers' parts will hold the output state to what it was when RESET is taken low, others will send the output either high or low.

**Phase-locked loop**

A phase detector compares two input signals and produces an error signal which is proportional to their phase difference. The error signal is then low-pass filtered and used to drive a VCO which creates an output phase. The output is fed through an optional divider back to the input of the system, producing a negative feedback loop. If the output phase drifts, the error signal will increase, driving the VCO phase in the opposite direction so as to reduce the error. Thus the output phase is locked to the phase at the other input. This input is called the reference.

Analog phase locked loops are generally built with an analog phase detector, low pass filter and VCO placed in a negative feedback configuration. A digital phase locked loop uses a digital phase detector; it may also have a divider in the feedback path or in the reference path, or both, in order to make the PLL's output signal frequency a rational multiple of the reference frequency. A non-integer multiple of the reference frequency can also be created by replacing the simple divide-by-N counter in the feedback path with a programmable pulse swallowing counter. This technique is usually referred to as a fractional-N synthesizer or fractional-N PLL.\[ dubious – discuss\]

Digital phase-locked loop block diagram
The oscillator generates a periodic output signal. Assume that initially the oscillator is at nearly the same frequency as the reference signal. If the phase from the oscillator falls behind that of the reference, the phase detector changes the control voltage of the oscillator so that it speeds up. Likewise, if the phase creeps ahead of the reference, the phase detector changes the control voltage to slow down the oscillator. Since initially the oscillator may be far from the reference frequency, practical phase detectors may also respond to frequency differences, so as to increase the lock-in range of allowable inputs.

Depending on the application, either the output of the controlled oscillator, or the control signal to the oscillator, provides the useful output of the PLL system.

**Analog to Digital Converter**

An analog-to-digital converter (abbreviated ADC, A/D or A to D) is a device that converts a continuous physical quantity (usually voltage) to a digital number that represents the quantity's amplitude.

The conversion involves quantization of the input, so it necessarily introduces a small amount of error. Instead of doing a single conversion, an ADC often performs the conversions ("samples" the input) periodically. The result is a sequence of digital values that have converted a continuous-time and continuous-amplitude analog signal to a discrete-time and discrete-amplitude digital signal.

**Resolution**

![Fig. 1. An 8-level ADC coding scheme.](image)

The resolution of the converter indicates the number of discrete values it can produce over the range of analog values. The resolution determines the magnitude of the quantization error and therefore determines the maximum possible average signal to noise ratio for an ideal ADC without the use of oversampling. The values are usually stored electronically in binary form, so the resolution is usually expressed in bits. In consequence, the number of discrete values available, or "levels", is assumed to be a power of two. For example, an ADC with a resolution of 8 bits can encode an analog input to one in 256 different levels, since $2^8 = 256$. The values can
represent the ranges from 0 to 255 (i.e. unsigned integer) or from −128 to 127 (i.e. signed integer), depending on the application.

Resolution can also be defined electrically, and expressed in volts. The minimum change in voltage required to guarantee a change in the output code level is called the least significant bit (LSB) voltage. The resolution $Q$ of the ADC is equal to the LSB voltage. The voltage resolution of an ADC is equal to its overall voltage measurement range divided by the number of discrete values:

$$Q = \frac{E_{FSR}}{2^M - 1}$$

where $M$ is the ADC's resolution in bits and $E_{FSR}$ is the full scale voltage range (also called 'span'). $E_{FSR}$ is given by

$$E_{FSR} = V_{RefHi} - V_{RefLow},$$

where $V_{RefHi}$ and $V_{RefLow}$ are the upper and lower extremes, respectively, of the voltages that can be coded.

Normally, the number of voltage intervals is given by

$$N = 2^M - 1,$$

where $M$ is the ADC's resolution in bits.\(^1\)

That is, one voltage interval is assigned in between two consecutive code levels.

**Quantization error**

Quantization error is the noise introduced by quantization in an ideal ADC. It is a rounding error between the analog input voltage to the ADC and the output digitized value. The noise is non-linear and signal-dependent.

In an ideal analog-to-digital converter, where the quantization error is uniformly distributed between $-1/2$ LSB and $+1/2$ LSB, and the signal has a uniform distribution covering all quantization levels, the Signal-to-quantization-noise ratio (SQNR) can be calculated from

$$SQNR = 20 \log_{10}(2^Q) \approx 6.02 \cdot Q \text{ dB}$$

Where $Q$ is the number of quantization bits. For example, a 16-bit ADC has a maximum signal-to-noise ratio of $6.02 \times 16 = 96.3$ dB, and therefore the quantization error is 96.3 dB below the maximum level. Quantization error is distributed from DC to the Nyquist frequency, consequently if part of the ADC's bandwidth is not used (as in oversampling), some of the quantization error will fall out of band, effectively improving the SQNR. In an oversampled system, noise shaping can be used to further increase SQNR by forcing more quantization error out of the band.
Accuracy

An ADC has several sources of errors. Quantization error and (assuming the ADC is intended to be linear) non-linearity are intrinsic to any analog-to-digital conversion.

These errors are measured in a unit called the least significant bit (LSB). In the above example of an eight-bit ADC, an error of one LSB is 1/256 of the full signal range, or about 0.4%.

ADC types

These are the most common ways of implementing an electronic ADC:

- A **direct-conversion ADC** or **flash ADC** has a bank of comparators sampling the input signal in parallel, each firing for their decoded voltage range. The comparator bank feeds a logic circuit that generates a code for each voltage range. Direct conversion is very fast, capable of gigahertz sampling rates, but usually has only 8 bits of resolution or fewer, since the number of comparators needed, $2^N - 1$, doubles with each additional bit, requiring a large, expensive circuit. ADCs of this type have a large die size, a high input capacitance, high power dissipation, and are prone to produce glitches at the output (by outputting an out-of-sequence code). Scaling to newer submicrometre technologies does not help as the device mismatch is the dominant design limitation. They are often used for video, wideband communications or other fast signals in optical storage.

- A **successive-approximation ADC** uses a comparator to successively narrow a range that contains the input voltage. At each successive step, the converter compares the input voltage to the output of an internal digital to analog converter which might represent the midpoint of a selected voltage range. At each step in this process, the approximation is stored in a successive approximation register (SAR). For example, consider an input voltage of 6.3 V and the initial range is 0 to 16 V. For the first step, the input 6.3 V is compared to 8 V (the midpoint of the 0–16 V range). The comparator reports that the input voltage is less than 8 V, so the SAR is updated to narrow the range to 0–8 V. For the second step, the input voltage is compared to 4 V (midpoint of 0–8). The comparator reports the input voltage is above 4 V, so the SAR is updated to reflect the input voltage is in the range 4–8 V. For the third step, the input voltage is compared with 6 V (halfway between 4 V and 8 V); the comparator reports the input voltage is greater than 6 volts, and search range becomes 6–8 V. The steps are continued until the desired resolution is reached.

- A **ramp-compare ADC** produces a saw-tooth signal that ramps up or down then quickly returns to zero. When the ramp starts, a timer starts counting. When the ramp voltage matches the input, a comparator fires, and the timer's value is recorded. Timed ramp converters require the least number of transistors. The ramp time is sensitive to temperature because the circuit generating the ramp is often just some simple oscillator. There are two solutions: use a clocked counter driving a DAC and then use the comparator to preserve the counter's value, or calibrate the timed ramp. A special advantage of the ramp-compare system is that comparing a second signal just requires another comparator, and another register to store the voltage value. A very simple (non-linear) ramp-converter can be implemented with a microcontroller and one resistor and capacitor. Vice versa, a filled capacitor can be taken from an integrator, time-to-amplitude converter, phase detector, sample and hold circuit, or peak and hold circuit and
discharged. This has the advantage that a slow comparator cannot be disturbed by fast input changes.

- **An integrating ADC** (also dual-slope or multi-slope ADC) applies the unknown input voltage to the input of an integrator and allows the voltage to ramp for a fixed time period (the run-up period). Then a known reference voltage of opposite polarity is applied to the integrator and is allowed to ramp until the integrator output returns to zero (the run-down period). The input voltage is computed as a function of the reference voltage, the constant run-up time period, and the measured run-down time period. The run-down time measurement is usually made in units of the converter's clock, so longer integration times allow for higher resolutions. Likewise, the speed of the converter can be improved by sacrificing resolution. Converters of this type (or variations on the concept) are used in most digital voltmeters for their linearity and flexibility.

- **A delta-encoded ADC** or **counter-ramp** has an up-down counter that feeds a digital to analog converter (DAC). The input signal and the DAC both go to a comparator. The comparator controls the counter. The circuit uses negative feedback from the comparator to adjust the counter until the DAC's output is close enough to the input signal. The number is read from the counter. Delta converters have very wide ranges and high resolution, but the conversion time is dependent on the input signal level, though it will always have a guaranteed worst-case. Delta converters are often very good choices to read real-world signals. Most signals from physical systems do not change abruptly. Some converters combine the delta and successive approximation approaches; this works especially well when high frequencies are known to be small in magnitude.

### Applications

#### Music recording

Analog-to-digital converters are integral to current music reproduction technology. People produce much music on computers using an analog recording and therefore need analog-to-digital converters to create the pulse-code modulation (PCM) data streams that go onto compact discs and digital music files.

The current crop of analog-to-digital converters utilized in music can sample at rates up to 192 kilohertz. Considerable literature exists on these matters, but commercial considerations often play a significant role. Most high-profile recording studios record in 24-bit/192-176.4 kHz pulse-code modulation (PCM) or in Direct Stream Digital (DSD) formats, and then downsample or decimate the signal for Red-Book CD production (44.1 kHz) or to 48 kHz for commonly used for radio and television broadcast applications.

#### Digital signal processing

People must use ADCs to process, store, or transport virtually any analog signal in digital form. TV tuner cards, for example, use fast video analog-to-digital converters. Slow on-chip 8, 10, 12, or 16 bit analog-to-digital converters are common in microcontrollers. Digital storage oscilloscopes need very fast analog-to-digital converters, also crucial for software defined radio and their new applications.

#### Scientific instruments

Digital imaging systems commonly use analog-to-digital converters in digitizing pixels.
Some radar systems commonly use analog-to-digital converters to convert signal strength to digital values for subsequent signal processing. Many other in situ and remote sensing systems commonly use analogous technology.

The number of binary bits in the resulting digitized numeric values reflects the resolution, the number of unique discrete levels of quantization (signal processing). The correspondence between the analog signal and the digital signal depends on the quantization error. The quantization process must occur at an adequate speed, a constraint that may limit the resolution of the digital signal.

Many sensors produce an analog signal; temperature, pressure, pH, light intensity etc. All these signals can be amplified and fed to an ADC to produce a digital number proportional to the input signal.

Digital-to-analog converter

In electronics, a digital-to-analog converter (DAC or D-to-A) is a device that converts a digital (usually binary) code to an analog signal (current, voltage, or electric charge). An analog-to-digital converter (ADC) performs the reverse operation. Signals are easily stored and transmitted in digital form, but a DAC is needed for the signal to be recognized by human senses or other non-digital systems.

A common use of digital-to-analog converters is generation of audio signals from digital information in music players. Digital video signals are converted to analog in televisions and mobile phones to display colors and shades. Digital-to-analog conversion can degrade a signal, so conversion details are normally chosen so that the errors are negligible.

Due to cost and the need for matched components, DACs are almost exclusively manufactured on integrated circuits (ICs). There are many DAC architectures which have different advantages and disadvantages. The suitability of a particular DAC for an application is determined by a variety of measurements including speed and resolution.

DAC types

The most common types of electronic DACs are:

- The pulse-width modulator, the simplest DAC type. A stable current or voltage is switched into a low-pass analog filter with a duration determined by the digital input code. This technique is often used for electric motor speed control, but has many other applications as well.
- Oversampling DACs or interpolating DACs such as the delta-sigma DAC, use a pulse density conversion technique. The oversampling technique allows for the use of a lower resolution DAC internally. A simple 1-bit DAC is often chosen because the oversampled result is inherently linear. The DAC is driven with a pulse-density modulated signal, created with the use of a low-pass filter, step nonlinearity (the actual 1-bit DAC), and negative feedback loop, in a technique called delta-sigma modulation. This results in an effective high-pass filter acting on the quantization (signal processing) noise, thus steering this noise out of the low frequencies of interest into the megahertz frequencies of little interest, which is called noise shaping. The quantization noise at these high frequencies is removed or greatly attenuated by use of an analog low-pass filter at the output (sometimes
a simple RC low-pass circuit is sufficient). Most very high resolution DACs (greater than 16 bits) are of this type due to its high linearity and low cost. Higher oversampling rates can relax the specifications of the output low-pass filter and enable further suppression of quantization noise. Speeds of greater than 100 thousand samples per second (for example, 192 kHz) and resolutions of 24 bits are attainable with delta-sigma DACs. A short comparison with pulse-width modulation shows that a 1-bit DAC with a simple first-order integrator would have to run at 3 THz (which is physically unrealizable) to achieve 24 meaningful bits of resolution, requiring a higher-order low-pass filter in the noise-shaping loop. A single integrator is a low-pass filter with a frequency response inversely proportional to frequency and using one such integrator in the noise-shaping loop is a first order delta-sigma modulator. Multiple higher order topologies (such as MASH) are used to achieve higher degrees of noise-shaping with a stable topology.

- The binary-weighted DAC, which contains individual electrical components for each bit of the DAC connected to a summing point. These precise voltages or currents sum to the correct output value. This is one of the fastest conversion methods but suffers from poor accuracy because of the high precision required for each individual voltage or current. Such high-precision components are expensive, so this type of converter is usually limited to 8-bit resolution or less.[citation needed]
  - Switched resistor DAC contains a parallel resistor network. Individual resistors are enabled or bypassed in the network based on the digital input.
  - Switched current source DAC, from which different current sources are selected based on the digital input.
  - Switched capacitor DAC contains a parallel capacitor network. Individual capacitors are connected or disconnected with switches based on the input.
- The R-2R ladder DAC which is a binary-weighted DAC that uses a repeating cascaded structure of resistor values R and 2R. This improves the precision due to the relative ease of producing equal valued-matched resistors (or current sources). However, wide converters perform slowly due to increasingly large RC-constants for each added R-2R link.
- The Successive-Approximation or Cyclic DAC, which successively constructs the output during each cycle. Individual bits of the digital input are processed each cycle until the entire input is accounted for.
- The thermometer-coded DAC, which contains an equal resistor or current-source segment for each possible value of DAC output. An 8-bit thermometer DAC would have 255 segments, and a 16-bit thermometer DAC would have 65,535 segments. This is perhaps the fastest and highest precision DAC architecture but at the expense of high cost. Conversion speeds of >1 billion samples per second have been reached with this type of DAC.
- Hybrid DACs, which use a combination of the above techniques in a single converter. Most DAC integrated circuits are of this type due to the difficulty of getting low cost, high speed and high precision in one device.
  - The segmented DAC, which combines the thermometer-coded principle for the most significant bits and the binary-weighted principle for the least significant bits. In this way, a compromise is obtained between precision (by the use of the thermometer-coded principle) and number of resistors or current sources (by the use of the binary-weighted principle). The full binary-weighted design means 0% segmentation, the full thermometer-coded design means 100% segmentation.
- Most DACs, shown earlier in this list, rely on a constant reference voltage to create their output value. Alternatively, a multiplying DAC[1] takes a variable input voltage for their
conversion. This puts additional design constraints on the bandwidth of the conversion circuit.

**DAC performance**

DACs are very important to system performance. The most important characteristics of these devices are:

**Resolution**

The number of possible output levels the DAC is designed to reproduce. This is usually stated as the number of bits it uses, which is the base two logarithm of the number of levels. For instance a 1 bit DAC is designed to reproduce 2 \(2^1\) levels while an 8 bit DAC is designed for 256 \(2^8\) levels. Resolution is related to the effective number of bits which is a measurement of the actual resolution attained by the DAC. Resolution determines color depth in video applications and audio bit depth in audio applications.

**Maximum sampling rate**

A measurement of the maximum speed at which the DACs circuitry can operate and still produce the correct output. As stated in the Nyquist–Shannon sampling theorem defines a relationship between the sampling frequency and bandwidth of the sampled signal.

**Monotonicity**

The ability of a DAC's analog output to move only in the direction that the digital input moves (i.e., if the input increases, the output doesn't dip before asserting the correct output.) This characteristic is very important for DACs used as a low frequency signal source or as a digitally programmable trim element.

**Total harmonic distortion and noise (THD+N)**

A measurement of the distortion and noise introduced to the signal by the DAC. It is expressed as a percentage of the total power of unwanted harmonic distortion and noise that accompany the desired signal. This is a very important DAC characteristic for dynamic and small signal DAC applications.

**Dynamic range**

A measurement of the difference between the largest and smallest signals the DAC can reproduce expressed in decibels. This is usually related to resolution and noise floor.

Other measurements, such as phase distortion and jitter, can also be very important for some applications, some of which (e.g. wireless data transmission, composite video) may even rely on accurate production of phase-adjusted signals.

Linear PCM audio sampling usually works on the basis of each bit of resolution being equivalent to 6 decibels of amplitude (a 2x increase in volume or precision).
Non-linear PCM encodings (A-law / μ-law, ADPCM, NICAM) attempt to improve their effective dynamic ranges by a variety of methods - logarithmic step sizes between the output signal strengths represented by each data bit (trading greater quantisation distortion of loud signals for better performance of quiet signals).

**Applications**

![A simplified functional diagram of an 8-bit DAC](image)

**Audio**

Most modern audio signals are stored in digital form (for example MP3s and CDs) and in order to be heard through speakers they must be converted into an analog signal. DACs are therefore found in CD players, digital music players, and PC sound cards.

Specialist standalone DACs can also be found in high-end hi-fi systems. These normally take the digital output of a compatible CD player or dedicated transport (which is basically a CD player with no internal DAC) and convert the signal into an analog line-level output that can then be fed into an amplifier to drive speakers.

Similar digital-to-analog converters can be found in digital speakers such as USB speakers, and in sound cards.

In VoIP (Voice over IP) applications, the source must first be digitized for transmission, so it undergoes conversion via an Analog-to-Digital Converter, and is then reconstructed into analog using a DAC on the receiving party's end.

![Top-loading CD player and external digital-to-analog converter.](image)
Video

Video sampling tends to work on a completely different scale altogether thanks to the highly nonlinear response both of cathode ray tubes (for which the vast majority of digital video foundation work was targeted) and the human eye, using a "gamma curve" to provide an appearance of evenly distributed brightness steps across the display's full dynamic range - hence the need to use RAMDACs in computer video applications with deep enough colour resolution to make engineering a hardcoded value into the DAC for each output level of each channel impractical (e.g. an Atari ST or Sega Genesis would require 24 such values; a 24-bit video card would need 768...). Given this inherent distortion, it is not unusual for a television or video projector to truthfully claim a linear contrast ratio (difference between darkest and brightest output levels) of 1000:1 or greater, equivalent to 10 bits of audio precision even though it may only accept signals with 8-bit precision and use an LCD panel that only represents 6 or 7 bits per channel.

Video signals from a digital source, such as a computer, must be converted to analog form if they are to be displayed on an analog monitor. As of 2007, analog inputs were more commonly used than digital, but this changed as flat panel displays with DVI and/or HDMI connections became more widespread. A video DAC is, however, incorporated in any digital video player with analog outputs. The DAC is usually integrated with some memory (RAM), which contains conversion tables for gamma correction, contrast and brightness, to make a device called a RAMDAC.

A device that is distantly related to the DAC is the digitally controlled potentiometer, used to control an analog signal digitally.

Mechanical

An unusual application of digital-to-analog conversion was the whiffletree electromechanical digital-to-analog converter linkage in the IBM Selectric typewriter.